Confirmation No. 9255

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	STEINBUSCH	Examiner:	Merant, G.
Serial No.:	10/539,104	Group Art Unit:	2117
Filed:	June 15, 2005	Docket No.:	US020610US2
Title:	CONNECTING MULTIPLE TEST ACCESS PORT CONTROLLERS ON A SINGLE TEST ACCESS PORT		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this communication is being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 29, 2007.

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APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner For Patents
P.O. Box 1450
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Customer No. 65913

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed June 30, 2007 and in response to the rejections of claims 1-15 as set forth in the Final Office Action dated April 2, 2007, and in further response to the Advisory Action dated June 13, 2007.

Please charge Deposit Account number 50-0996 (NXPS.211PA) $500.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

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I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 017329/0899 to Koninklijke Philips Electronics, N.V., headquartered in Eindhoven, the Netherlands. We have been authorized by both the assignee of record and NXP Semiconductors to convey herein that the entire right, title and interest of the instant patent application has been transferred to NXP Semiconductors.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-15 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Office Action dated April 2, 2007.

V. Summary of Claimed Subject Matter

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a method of coupling a plurality of test access port (TAP) controllers (*e.g.*, elements 102 and 106 of FIG. 3) to a single external interface(*e.g.*, paragraphs 24 and 30), comprising: a) resetting a first bit in each of a plurality of TAP controllers to a known state (*e.g.*, paragraph 35 and element 602 of FIG. 6); b) producing a first signal based, at least in part, on the state of the first bit in each of the plurality of TAP controllers (*e.g.*, paragraph 35 and element 604 of FIG. 6); c) selecting one of the plurality of TAP controllers based, at least in part, on the first signal (*e.g.*, paragraph 35 and element 606 of FIG. 6); d) coupling an external input terminal to an input terminal of the selected one of the plurality of

TAP controllers (*e.g.*, paragraph 30); and e) coupling an output terminal of the selected one of the plurality of TAP controllers to an external output terminal (*e.g.*, paragraph 30).

Commensurate with independent claim 8, an example embodiment of the present invention is directed to an integrated circuit, comprising: a plurality of functional blocks, each functional block having a test access port (TAP) controller (*e.g.*, elements 102 and 106 of FIG. 3) coupled thereto; each TAP controller including a first register bit (*e.g.*, element 212 of FIG. 2), each first register bit adapted to produce a known output state in response to a reset signal (*e.g.*, paragraph 37), each first register bit further adapted to toggle in response to a register write operation (*e.g.*, paragraph 31); and routing logic adapted to selectively provide, based at least in part on the state of the plurality of first register bits, a communication path between an external input signal source and an input terminal of a selected one of the TAP controllers (*e.g.*, paragraph 27 and FIG. 1).

Commensurate with independent claim 12, an example embodiment of the present invention is directed to an integrated circuit (IC), comprising: a plurality of test access port (TAP) controllers (*e.g.*, elements 102 and 106 of FIG. 3) disposed on the IC, each of the plurality of TAP controllers having a first input terminal adapted to receive a data input signal and an output terminal adapted to provide a data output signal (*e.g.*, paragraph 27 and FIG. 1), each of the plurality of TAP controllers further having at least one switch bit (*e.g.*, element 212 of FIG. 2); a first interface to receive an externally supplied input signal; a second interface to transmit an internally generated output signal; and routing logic adapted to selectively provide, based at least in part on the state of the switch bits of the plurality of TAP controllers, a first communication path between the input terminal of a predetermined one of the plurality of TAP controllers and the first interface, and a second communication path between the output terminal and the second interface (*e.g.*, paragraphs 27-30 and FIG. 1).

VI. Grounds of Rejection to be Reviewed Upon Appeal

A. Whether claims 1-15 are unpatentable under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,311,302 to Cassetti *et al.* (Cassetti).

VII. Argument

A. The rejections of Claims 1-15 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,311,302 to Cassetti *et al.* (Cassetti)

i. The rejections are improper because Cassetti reference does not teach each claim limitation.

The record clearly shows that the Cassetti reference does not teach the limitations directed toward setting a bit in a TAP controller. The law and M.P.E.P are clear in that M.P.E.P. 2111.01 states that the claim terms must be given their ordinary and customary meaning. See *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313. Moreover, even the plain meaning of a term cannot be inconsistent with the specification. See *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). The Examiner appears to be confusing similarly named, yet distinct, components in a manner that both runs afoul of the ordinary and customary meaning and is inconsistent with Appellant's specification.

More specifically, the Examiner fails to acknowledge the differences between a TAP controller, a chip-level TAP link Module and a test link module (TLM). There is no dispute in the record that a TAP controller is understood in the context of the functionality defined by various IEEE specifications. The record provides a specific example of such functionality as shown by the state diagram of FIG. 14 of U.S. Patent No. 6,073,254 to Whetsel[1]. Accordingly, one of skill in the art would recognize that the standard-compliant TAP Controller is finite state machine that controls a JTAG scan through control of its current state via its initial state and the subsequent sequence of TMS signals received. *See, e.g.*, U.S. Letters Patent 5,627,842 to Brown *et al.* at Col. 5, lines 8-32.[2] The record also provides context for various terms, such as TAP controller and TAP Link Module, in U.S. Patent No. 6,385,749 to Adusumilli, *et al.*[3] This usage is also inconsistent with the Examiner's interpretation. A word search of the U.S. Patent Database also reveals usage of the term test link module that is inconsistent with the Examiner's interpretation. Accordingly, there is a

[1] As provided in the Examiner's Notice of Cited references dated April 2, 2007.
[2] As provided in Applicant's IDS statement dated June 15, 2005.
[3] As provided in the Examiner's Notice of Reference Cited dated October 20, 2006.

clear distinction between the functionality of such TAP controllers and the test link module of the Cassetti reference. More specifically, TAP controllers provide a mechanism (*e.g.*, state machine) to implement a JTAG scan in response to the TMS signal. The test link module provides a mechanism that alternates when a TMS signal is provided to each of the TAP controllers. See, e.g., Cassetti at Col. 5, line 7 *et al.* The distinction between these elements may become more apparent through an analysis of a simple replacement of the test link module 12 of the Cassetti reference by a TAP controller as defined by the record (including the Cassetti reference). Such an analysis reveals that the TAP controller would fail to provide a mechanism to alternate the TMS signal between TAP controllers 16 and 18. Accordingly, the Examiner's interpretation results in an illogical result in which the Cassetti reference would fail to function.

Moreover, both Appellant's disclosure (*see, e.g.*, paragraph 24 of Appellant's disclosure) and the Cassetti reference (*see, e.g.*, Cassetti at Col. 2, lines 7-51 and at Col. 4, lines 12-24) are consistent in defining a chip level TAP Link Module and a test link module as elements that provide control for multiple TAP controllers. As such, both of these modules are distinct from the TAP controllers for which these modules provide control. A close look at FIG. 1 of the Cassetti reference further clarifies this distinction. For example, chip level TAP link module 40 is distinct from and provides control for two test link modules 12 and 14. Test link modules 12 and 14 are distinct from and provide control to TAP controllers 16, 18, 30 and 32. Accordingly, there is no basis in the record for the Examiner's interpretation, which is inconsistent with the plain usage of the relevant terms in view of the record.

Moreover, the Examiner's interpretation is inconsistent with the usage of the term "TAP controller" by Appellant's specification. Claim limitations should not be imported from the specification. When possible, however, claim terms should be interpreted in a manner that is consistent with the usage therein. More specifically, the meaning of a particular claim term may be defined by implication, that is, according to the usage of the term in the context in the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). In this instance, the Examiner's interpretation of a TAP controller is

inconsistent with (and finds no support based upon) the usage of the term within Appellant's specification.

The Examiner relies upon the bit stored within Cassetti's test link module 12 of FIG. 1. As discussed above, the record clearly shows that this bit is not stored within the TAP controllers 16 or 18. The claim limitations require that the register bit is in the TAP controller. (Claim 1: "resetting a first bit in each of a plurality of TAP controllers to a known state"). Thus, the interpretation that would arguably meet the above mentioned limitations is one in which the test link module 12 is the TAP controller. The application of this interpretation to various other claim limitations produces an illogical result that is inconsistent with Appellant's specification. For instance, the test link module 12 enables the other test link module by passing data (*e.g.*, using the TMS, Capture, Shift and Update signals) to a chip level tap link module 40. See, e.g., Cassetti at Col. 5, line 7 *et al.* Appellant's specification provides inconsistent embodiments of Appellant's invention that, but for this interpretation, would be consistent. For instance, some embodiments disclose that no additional controllers (*e.g.*, TAP Linking Module) are needed to force a particular mode of operation. *See, e.g.*, Appellant's Specification at paragraph 24. Moreover, Appellant specification does not disclose any embodiment having placement of the bit in a manner that could be construed as equivalent to the placement of the asserted bit of the Cassetti reference (*i.e.*, a bit that is external to two tap controllers for control thereof). Thus, the Examiner's interpretation of the term "TAP controller" is inconsistent with the usage of the term in Appellant's specification.

The record is clear that a proper interpretation of a TAP controller would exclude equating either a test link module or a TAP Link Module thereto. In direct contradiction, however, the Examiner's interpretation of the Cassetti reference requires that test link modules 12 and 14 be equivalent to a TAP controller. In view of the record, which includes Appellant's disclosure, the Cassetti reference and several U.S. Letters Patents, one of skill in the art would understand that a TAP controller is not equivalent to test link modules 12 and 14. Moreover, the record shows that the claim term has been improperly interpreted in a manner that is inconsistent with Appellant's specification. Accordingly, the Cassetti reference fails to teach or suggest each claim limitation, including the claim limitations

directed to the setting and usage of a bit in a TAP controller. In view of this improper interpretation by the Examiner and the resulting lack of correspondence, the rejections are improper and must be reversed.

The rejections are also improper because the Examiner has improperly pieced together different portions of the cited Cassetti reference without showing how these portions work together to arrive at the claimed limitations. The law is clear in this matter, as indicated by Section 2131 of the M.P.E.P. "the identical invention must be shown in as complete detail as is contained in the ... claim" (citing *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1239 (Fed Cir. 1989). M.P.E.P. § 2131 further states that various portions of a reference cannot be asserted together to anticipate a claim unless the reference arranges the limitations as they are arranged in the claim.

Specifically, the Examiner cites to various portions of the Cassetti reference that relate to a first circuit (*e.g.*, FIG. 1) as allegedly corresponding to several of the claimed limitations. *See, e.g.,* Figure 1, Col. 3:6-19, Col. 6:1-10 and Col. 4:53-65. The Examiner then cites to the Background of the Cassetti reference as supposedly corresponding to claimed limitations directed to producing a first signal based at least in part on the state of the first bits in the TAP controllers. *See, e.g.,* Col. 2:21-50. As is indicated by the Cassetti reference, this portion of the Background discusses the teachings of U.S. patent application, Ser. No. 09/283,171. *See, e.g.,* Col. 2:30-37. Thus, the Examiner appears to be combining two different circuits/applications. The Examiner has not provided any rationale for combining these circuits nor shown how such a combination could function. In failing to cite any portion of the Cassetti reference that shows all of the limitations arranged as claimed in the instant application, the Examiner has failed to show correspondence to the claimed limitations in a manner consistent with M.P.E.P. § 2131. In this regard, the Examiner fails to provide correspondence to the claimed limitations and the Section 102(b) rejection of claims 1-15 should be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-15 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/538,104)

1. A method of coupling a plurality of test access port (TAP) controllers to a single external interface, comprising:

a) resetting a first bit in each of a plurality of TAP controllers to a known state;

b) producing a first signal based, at least in part, on the state of the first bit in each of the plurality of TAP controllers;

c) selecting one of the plurality of TAP controllers based, at least in part, on the first signal;

d) coupling an external input terminal to an input terminal of the selected one of the plurality of TAP controllers; and

e) coupling an output terminal of the selected one of the plurality of TAP controllers to an external output terminal.

2. The method of claim 1, wherein the TAP controller comprises a finite state machine and a plurality of registers.

3. The method of claim 2, further comprising toggling the first bit in the selected one of the plurality of TAP controllers; and repeating steps (b) through (e).

4. The method of claim 3, further comprising providing a clock signal, a test mode selection signal, and a test reset signal to each of the plurality of TAP controllers.

5. The method of claim 3, wherein the plurality of TAP controllers are disposed on a single integrated circuit.

6. The method of claim 5, wherein the first signal is produced within the single integrated circuit.

7. The method of claim 6, further comprising receiving, from a source external to the single integrated circuit, a clock signal.

8. An integrated circuit, comprising:

a plurality of functional blocks, each functional block having a test access port (TAP) controller coupled thereto;

each TAP controller including a first register bit, each first register bit adapted to produce a known output state in response to a reset signal, each first register bit further adapted to toggle in response to a register write operation; and

routing logic adapted to selectively provide, based at least in part on the state of the plurality of first register bits, a communication path between an external input signal source and an input terminal of a selected one of the TAP controllers.

9. The integrated circuit of claim 8, wherein the routing logic is further adapted to selectively provide, based at least in part on the state of the plurality of first register bits, a communication path between an external output terminal and an output terminal of the selected on the TAP controllers.

10. The integrated circuit of claim 8, wherein at least one TAP controller further includes a second register bit; wherein the routing logic is further to provide the output of a first TAP controller as an input to a second TAP controller, based at least in part on the state of the first and second register bits.

11. The integrated circuit of claim 9, wherein a transition between the selectively provided communication paths is transparent to an external observer.

12. An integrated circuit (IC), comprising:

a plurality of test access port (TAP) controllers disposed on the IC, each of the plurality of TAP controllers having a first input terminal adapted to receive a data input signal and an output terminal adapted to provide a data output signal, each of the plurality of TAP controllers further having at least one switch bit;

a first interface to receive an externally supplied input signal;

a second interface to transmit an internally generated output signal; and

routing logic adapted to selectively provide, based at least in part on the state of the switch bits of the plurality of TAP controllers, a first communication path between the input terminal of a predetermined one of the plurality of TAP controllers and the first interface, and a second communication path between the output terminal and the second interface.

13. The integrated circuit of claim 12, further comprising a plurality of functional blocks coupled respectively to each of the plurality of TAP controllers.

14. The integrated circuit of claim 13, wherein the each of the plurality of TAP controllers has a second input terminal adapted to receive a clock signal, a third input terminal adapted to receive mode select signal, and a fourth input terminal adapted to receive a reset signal; wherein the plurality of second input terminals are coupled in common, the plurality of third input terminals are coupled in common, and the plurality of fourth input terminals are coupled in common.

15. The integrated circuit of claim 14, further comprising a chain bit disposed in a first one of the plurality of TAP controllers.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132. Appellant has attached copies of several U.S. Letters Patents. These patents were already part of the record and have been included in an abundance of caution. The attached U.S. Letters Patents include U.S. Patent Nos. 6,073,254 to Whetsel (Appendix A, 19 sheets), 5,627,842 to Brown *et al.* (Appendix B, 35 sheets), and 6,385,749 to Adusumilli, *et al.* (Appendix C, 14 sheets)

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.